

Electronic Acknowledgement Receipt

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International Application Number:	
Confirmation Number:	3824
Title of Invention:	METHODOLOGY AND APPLICATIONS OF TIMING-DRIVEN LOGIC RESYNSYNTHESIS FOR VLSI CIRCUITS
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
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1		APLUS001A_ISSUEPYMT.pdf	133843	yes	5				
	Multipart Description/PDF files in .zip description								
	Document Description		Start	End					
	Miscellaneous Incoming Letter		1	1					
	Issue Fee Payment (PTO-85B)		2	2					
	Miscellaneous Incoming Letter		3	3					
	Miscellaneous Incoming Letter		4	5					
Warnings:									
Information:									
2	Fee Worksheet (PTO-06)	fee-info.pdf	8200	no	2				
Warnings:									
Information:									
Total Files Size (in bytes):			142043						
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